



# ENIAC-on-a-Chip

BY JAN VAN DER SPIEGEL

**T**ake the ENIAC, an 80 by 3 foot giant, and shrink it to fit a silicon chip the size of your fingernail. Place the chip on a tiny circuit board. Connect the circuit board to a PC running graphical software simulating the ENIAC's look and feel. This is the recipe that students and faculty at the School of Engineering and Applied Science—with support from the National Science Foundation and Atmel Corporation—are using to create the ENIAC-on-a-Chip Kit, a teaching tool that dramatically illustrates the performance improvements brought about by semiconductor technology.

The chip preserves the ENIAC's original architecture and basic circuit building blocks as much as possible. To recreate the giant computer using modern technology, the ENIAC's 18,000 vacuum tubes and 170,000 resistors were modeled with 250,000 tiny transistors, mechanical switches were replaced with electronic ones, and digit and programming trunks were implemented as tiny metal lines interconnected through cross-point switches. The chip performs the same functions that its 30-ton predecessor pioneered 50 years ago. ENIAC-on-a-Chip includes the following units:

- 20 accumulators—the arithmetic workhorses, which also serve as memory elements
- constant transmitter—the module that allows initialization of the accumulators to a constant integer
- cycling unit—the master clock that synchronizes the operation of all modules
- initiation unit—the element that tells all modules when to start computation
- function table—the module that gives arbitrary functional dependence for the input
- master programmer—the higher level arithmetic coordinator that allows more sophisticated programming of the chip
- high-speed multiplier—the module that manipulates the accumulators to perform multiplication
- divider—the module that manipulates the accumulators to perform division
- square rooter—the module that manipulates the accumulators to perform square roots

The chip, fabricated in a technology whose smallest features are .8 micrometers, is due back from the silicon foundry in mid-April. Following is a comparison between the ENIAC and ENIAC-on-a-Chip:

	ENIAC	ENIAC-on-a Chip
Vacuum tubes	18,000	none
Transistors	none	250,000
Resistors	170,000	none
Capacitors	10,000	none
Footprint	80x3 ft	8x8 mm
Clock speed	100 kHz	20 MHz*
Power	174 kW	0.5 W*

\*estimated

Once back from the foundry, the chip will be mounted on a small, printed circuit board and connected to a PC. The PC will be equipped with a graphical interface that allows a user to interact with the chip. The interface will display the front panels of the the ENIAC with its programming switches, control switches, and interconnection cables (digit lines and programming lines). The user will select the switches to generate the proper program settings and interconnections to create a data file. The file will be sent to the chip and the output of the chip (lights indicating the output of the accumulators) will be read back into the PC for display, allowing the user to evaluate results.

The ENIAC-on-a-Chip Kit, consisting of chip, printed circuit board, PC software, and a set of demonstration programs (data files), will be available to a variety of organizations and institutions, including the National Science Foundation and the Smithsonian. The multidimensional educational and intellectual benefits of the kit will not only inspire students in engineering and science but will reach out to a larger audience ranging from historians to high school students and the public at large.

For more information about ENIAC-on-a-Chip, the Kit, and the student and faculty developers, see <http://www.ee.upenn.edu/~jan/eniacproj.html>.

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